REMARKS

Claims 1, 13 and 14 are currently pending. The amendment to claim 1 is explicitly supported at page 18, lines 19-21, as well as elsewhere. New claims 13 and 14 are supported by the full adders (FA) and half adders (HA) shown in Figures 3 and 6, for example, and the related text.

The Office Action of March 25, 2004 includes rejections of claim 1 under 35 U.S.C. § 112, first and second paragraphs, suggesting that the claim phrase "said plurality of adders include only a half adder and a full adder" is not supported in the specification. Applicants were attempting only to identify the type of circuits being used. However, the Examiner's comment is noted with appreciation and the claims have been reworded to arguably be broader, in light of his comments. Specifically, the phrase in question has been moved and divided into claims 13 and 14. Claim 13 now recites that the plurality of adders of each of first to *m*th digit calculating portions includes one half adder and at least one full adder. Claim 14 recites that the plurality of adders of each of first to *m*th digit calculating portions includes at least one full adder wherein the one full adder provides only one bit of additional output and one bit of carry output based only on two bits of data input and one bit of carry input. These recitations are supported by the specification by the full adders (e.g., FA23) by the two arrow lines show signals leading FA23 and three arrow lines showing inputs to FA23, and the text related thereto.

In light of these changes, Applicants respectfully request that the rejections based on 35 U.S.C. § 112, first and second paragraphs, be withdrawn.

The Office Action also includes a rejection of claim 1, as so far understood, under 35 U.S.C. § 102(b) as being anticipated by the Detroye patent (U.S. Patent No. 4,748,581). This rejection is respectfully traversed.

In the comments appearing on page 3 of the Office Action, the Examiner notes that he "does not compare the BOA, but only the full adder (FA) as the claimed adder." One of Applicants' basic points is that the Detroye patent uses controllable add/subtract cells which are more complicated than is necessary in light of the present invention. For instance, the Detroye patent shows four inputs to each BOA and apparently has problems similar to those described with reference to the prior art at pages 2 and 3 of the present application. It appears that the Office understands that the Controllable Add/Subtract (CAS) cells (identified as BOAs in the Detroye patent) are not the same as the present application which avoids the need for CAS cells. Accordingly, claim 1 has been amended to more directly recite novel features of the present invention, i.e., that the square root extraction circuit outputs binary square root data without using controllable add/subtract cells.

The Detroye patent clearly and unequivocally uses such cells and therefore does not anticipate claim 1, as amended. Applicants also note that claim 1 recited the use of an algorithm for determining the square root data "on the basis of said input data by only additions of square root partial data q(l)-q(m) in q(l) to q(m) order."

Applicants respectfully submit that claim 1 is neither anticipated nor rendered obvious by the prior art of record. It is noted that claims 13 and 14 are also not anticipated insofar claim 13 recited the use of half-adders not seen in the Detroye

patent, and claim 14 only requires three input bits of data, and not four as shown in the Detroye patent.

In light of the foregoing, Applicants respectfully request reconsideration and allowance of the above-captioned application. Should any residual issues exist, the Examiner is invited to contact the undersigned at the number listed below.

Respectfully submitted,

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